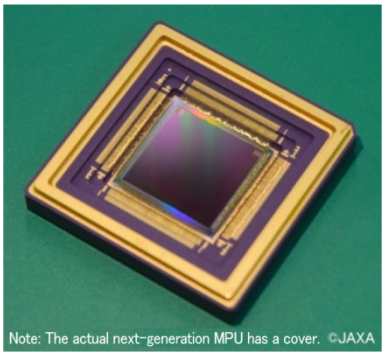
Development of Next-generation Space-grade Microprocessor



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*A microprocessor is a single integrated circuit on which functions, such as arithmetic and control, are implemented. In recent years, microprocessors equipped with a CPU, memory, communication interfaces etc., have been widely used in smartphones, automobiles, electric devices, etc. The microprocessor is also an indispensable component for spacecraft and is a strategic part that strengthens their competitiveness. The Japan Aerospace Exploration Agency (JAXA) has positioned space-use microprocessors as key components of the space industry and has been proceeding with their development. The "next-generation space-grade microprocessor (next-generation MPU)" presented in this report is the successor to the current space grade microprocessor, developed by JAXA. Mitsubishi Heavy Industries, Ltd. (MHI), on the other hand, has successfully developed space-use microprocessor (SOI-SOC2), by applying our patents related to radiation tolerance enhancement. And due to such capabilities, MHI was selected by JAXA to lead the development of next-generation MPU as the manufacturer (**Figure 1**). As of fiscal 2021, the development of the prototype has been completed and the design and manufacture of the flight model is in progress.*

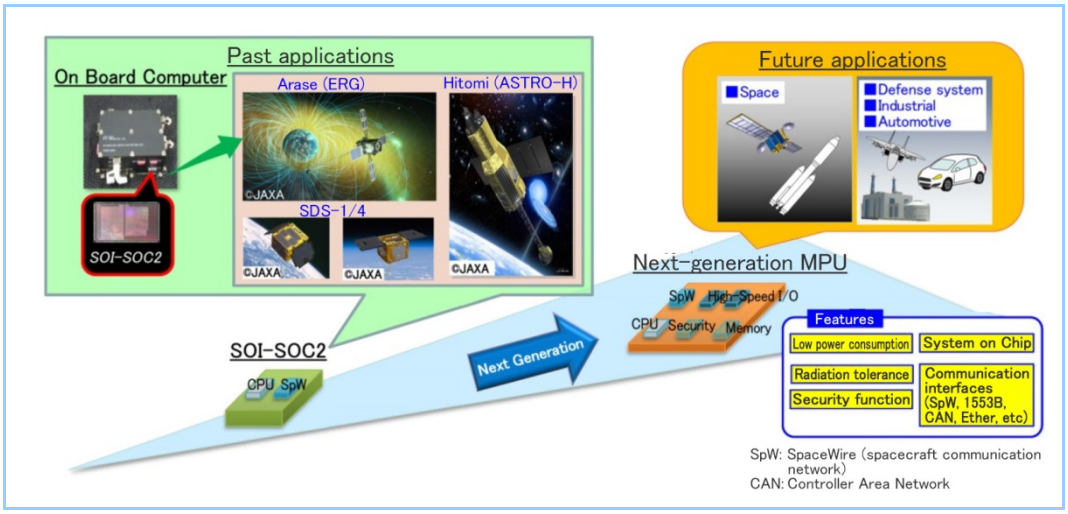


Figure 1 Roadmap for our space-grade microprocessor

1. Features

This chapter describes features of the next-generation MPU.

1.1 Low power consumption and high energy efficiency

Advanced commercial SOI (Silicon on Insulator) technology is used, which realizes the world's top level of processing performance per unit of power consumption. (For reference, the next-generation MPU attains 0.93 CoreMark®(Note 1)/mW and an overseas competitor product 0.56 CoreMark®/mW.)

1.2 Various communication interfaces and SoC (System on a Chip)

The next-generation MPU has a variety of built-in communication interfaces and can not only be used in the space field, but is also being considered for dual-use application (**Figure 1**). In addition, SoC design technology that enables multiple functions, including communication interfaces, memory, etc., mounted on to a single chip, contributes to cost reduction by reducing the number of parts in the entire system, as well as to the simplification of electronic board design.

The development specifications of the communication interfaces, internal memory capacity, etc., were determined based on opinions gathered from the next-generation MPU user group, in order to have better consistency with user needs compared to past development. The next-generation MPU user group, which is consisted by future potential users, was organized in the early stage of the development in collaboration with JAXA.

1.3 Security function

The following security functions are to be implemented on the next-generation MPU, in order to meet the demands of security requirements for spacecraft systems, etc. Security functions are considered to become more important in the future for the communication business using satellite constellations.

(1) Cryptographic processing

Utilizes various cryptographic algorithms to encrypt data and data origin authentication (including programs).

(2) Access control

A function to restrict unintended access (including unauthorized access) to information is implemented by hardware, to protect high-value data and confidential information.

1.4 Radiation tolerance

Based on the radiation hardened by design that we have acquired in the development of space-grade microprocessors (SOI-SOC2, etc.), radiation tolerance (Total Ionizing Dose, Single Event Error) required for space-grade microprocessors will be realized.

1.5 Operating system (OS)

A real-time OS with ITRON(Note 2) specifications will be developed in parallel with hardware to facilitate software development.

1.6 Development environment

An evaluation board (**Figure 2**) will be provided to support the initial introduction to customers. In addition, the use of e² studio produced by Renesas Electronics will be provided as an integrated development environment. This provides a development environment to immediately evaluate the developed item.

Note 1: CoreMark®: A benchmark developed by EEMBC (a non-profit industry group established for the purpose of formulating standard benchmarks for embedded systems) to measure the processing performance of CPUs.

Note 2: ITRON: An abbreviation for "Industrial TRON," which is the name of the real-time OS specification for embedded systems.

Figure 2 Evaluation bord (mounted with the next-generation MPU)

2. Specifications

Table 1 shows the outline of the next-generation MPU specifications and **Figure 3** shows the functional block diagram.

Table 1 Outline of next-generation MPU specifications

Item	Explanation
CPU	- Renesas RXv3 - Number of cores: Dual-core - FPU: Double-precision-FPU(IEEE-754)
Communication interfaces	- SpaceWire, MIL-STD-1553B - Ethernet*1 - CAN*2, SCI*2, SPI*2, I2C*2, GPIO*2, PWM*2
Internal memory	- SRAM with EDAC - Capacity: Code RAM: 4 MB*3, Shared RAM: 2 MB*3
External bus extension	- External bus controller - SDRAM controller with Reed-Solomon EDAC (Capacity: 512 MB*3, Throughput: 100 Mbps or more)
Security function	- Cryptographic processing: Data decryption by common key cryptography, data decryption by public key cryptography, hash value calculation and physical random number generation - Access control: Measure against modification targeting the boot sequence, restricting access to important data, measure against unauthorized access targeting cryptographic processing hardware, etc.
Package	- 572-pin Ceramic BGA (size: 26 mm × 26 mm)
Power supply voltage	- I/O: 3.3 V*4, Core: 1.2 V*4
Power consumption	- 1 W or less*5
Operating junction temperature	- -40°C to +125°C
Radiation tolerance	- TID: 100 krad or more - SEL: LET threshold 75 MeV/(mg/cm^2) or more - SEU: LET threshold 40 MeV/(mg/cm^2) or more*6

[Abbreviations]
FPU Floating Point Unit
CAN Controller Area Network
SCI Serial Communication Interface
SPI Serial Peripheral Interface
PWM Pulse Width Modulation
EDAC Error Detection And Correction
BGA Ball Grid Array
TID Total Ionizing Dose
SEL Single Event Latchup
SEU Single Event Upset
LET Linear Energy Transfer

*1 Uses Renesas Electronics IP (equivalent to product equipped with RZ A1H)
*2 Uses Renesas Electronics IP (equivalent to product equipped with RX64M/71M)
*3 Not including capacity reserved for EDAC
*4 Typical conditions
*5 Power supply voltage I/O: 3.3 V, Core: 1.2 V, Operating temperature: +25°C
*6 For reference, the error rate of the internal memory (Code RAM and Shared RAM) in orbit are as follows:
GEO (solar min): 7.27×10^{-7} errors/device/day, LEO (solar min): 3.30×10^{-8} errors/device/day

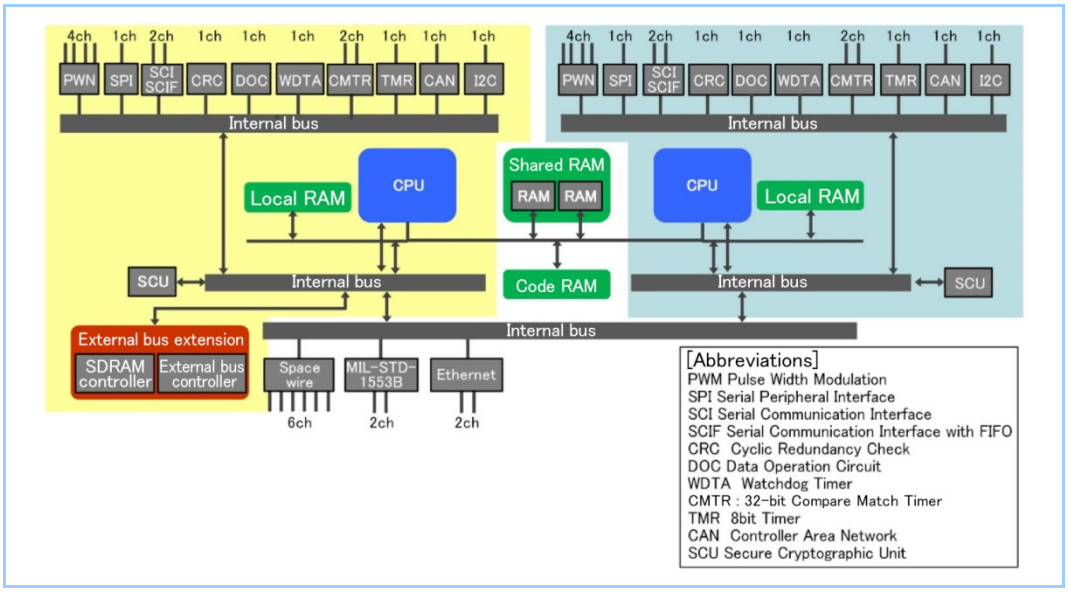


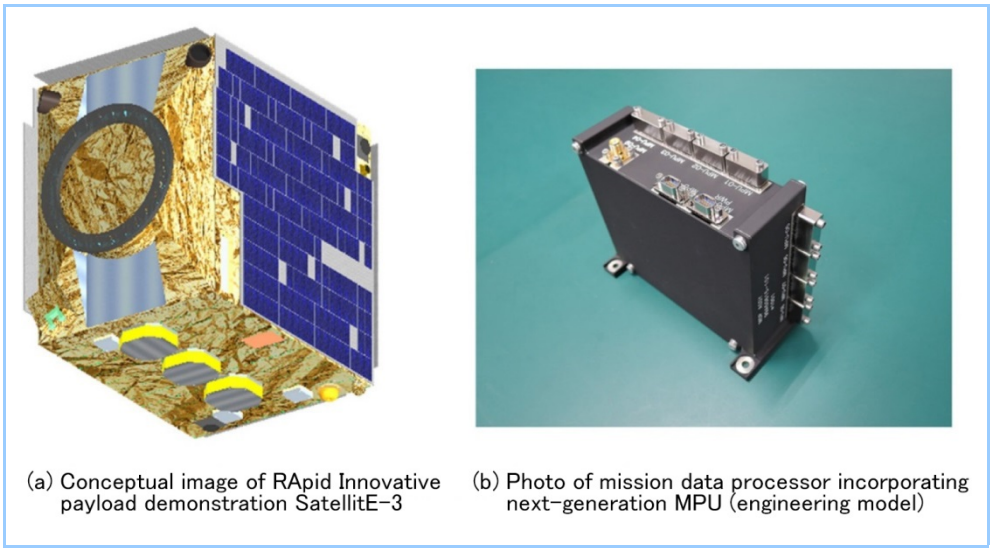
Figure 3 Functional block diagram of next-generation MPU

3. Future prospects

MHI has so far developed a prototype (engineering model) of the next-generation MPU and performed electrical function and performance evaluation tests, radiation tests and reliability evaluation tests. In the future, on-orbit demonstration using an engineering model is planned with the Innovative Satellite Technology Demonstoration-3, which is scheduled to be launched in fiscal 2022 (**Figure 4**). We have also started designing a flight model and will proceed with development toward production the engineering model and development environment (including the evaluation board) can be supplied as of October 2021. The flight model and OS will be supplied around the end of fiscal 2022.

The next-generation MPU is expected to be installed mainly on government-affiliated spacecraft such as JAXA satellites after the development of the flight model is completed. We are also looking to expand its use to NewSpace and dual-use applications in the future. As one such measure, we are conducting basic verification of low-priced package elemental technologies. Furthermore, in addition to selling the microprocessor, we are also considering the development of space-use electric components including this product such as mission data processors.

As mentioned at the beginning, the space-grade microprocessor is a key component that strengthens the competitiveness of Japanese spacecraft. We will contribute to the development of Japan's space science and space industry by providing a stable supply of next-generation MPUs.



(a) Conceptual image of RApid Innovative payload demonstration SatellitE-3

(b) Photo of mission data processor incorporating next-generation MPU (engineering model)

Figure 4 Conceptual image of RApid Innovative payload demonstration SatellitE-3 and photo of mission data processor incorporating next-generation MPU

References

(1) https://www.kenkai.jaxa.jp/research/soisoc/soisoc.html